

○ TRANSMISSION BIT ORDER (D0 TO D9 SHOW TRANSMITTED DATA, C4 TO C0 SHOW CRC BITS)

CONVENTIONAL POSTPOSITION : D9,D8,D7,D6,D5,D4,D3,D2,D1,D0,C4,C3,C2,C1,C0

PREPOSITION : C4,C3,C2,C1,C0,D9,D8,D7,D6,D5,D4,D3,D2,D1,D0

FIG.1A

○ RECEIVED DATA BIT AND RECEIVED CRC BIT
(WHEN DETECTING A POSITION WHERE THE NUMBER OF BITS IS
SMALLER BY ONE FROM THE CORRECT RATE POSITION)

CONVENTIONAL POSTPOSITION: DATA = D9,D8,D7,D6,D5,D4,D3,D2,D1 CRC=D0,C4,C3,C2,C1

PREPOSITION: DATA = D9,D8,D7,D6,D5,D4,D3,D2,D1 CRC=C4,C3,C2,C1,C0

FIG.1B

○TRANSMISSION BIT ORDER (D0 TO D9 SHOW TRANSMITTED DATA, C4 TO C0 SHOW CRC BITS)

CONVENTIONAL POSTPOSITION: D9,D8,D7,D6,D5,D4,D3,D2,D1,D0,C4,C3,C2,C1,C0

NEW POSTPOSITION: D9,D8,D7,D6,D5,D4,D3,D2,D1,D0,C0,C1,C2,C3,C4

FIG.2A

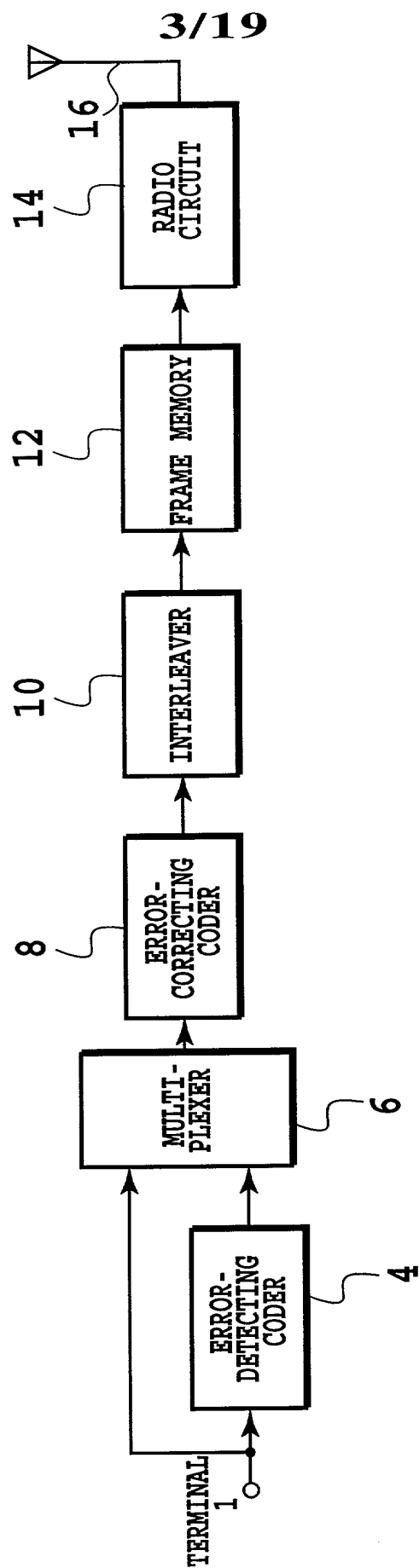
○RECEIVED DATA BIT AND RECEIVED CRC BIT
 (WHEN DETECTING A POSITION WHERE THE NUMBER OF BITS IS
 SMALLER BY ONE FROM THE CORRECT RATE POSITION)

CONVENTIONAL POSTPOSITION: DATA =D9,D8,D7,D6,D5,D4,D3,D2,D1 CRC=D0,C4,C3,C2,C1

NEW POSTPOSITION: DATA =D9,D8,D7,D6,D5,D4,D3,D2,D1 CRC=D0,C0,C1,C2,C3

FIG.2B

FIG. 3A is a block diagram of a transmitter configuration. The transmitter includes a terminal 1, an error detecting coder 4, a multi-plexer 6, an error correcting coder 8, an interleaver 10, a frame memory 12, and a radio circuit 14. The terminal 1 is connected to the error detecting coder 4. The error detecting coder 4 is connected to the multi-plexer 6. The multi-plexer 6 is connected to the error correcting coder 8. The error correcting coder 8 is connected to the interleaver 10. The interleaver 10 is connected to the frame memory 12. The frame memory 12 is connected to the radio circuit 14. The radio circuit 14 is connected to an antenna 16.



TRANSMITTER CONFIGURATION

FIG.3A

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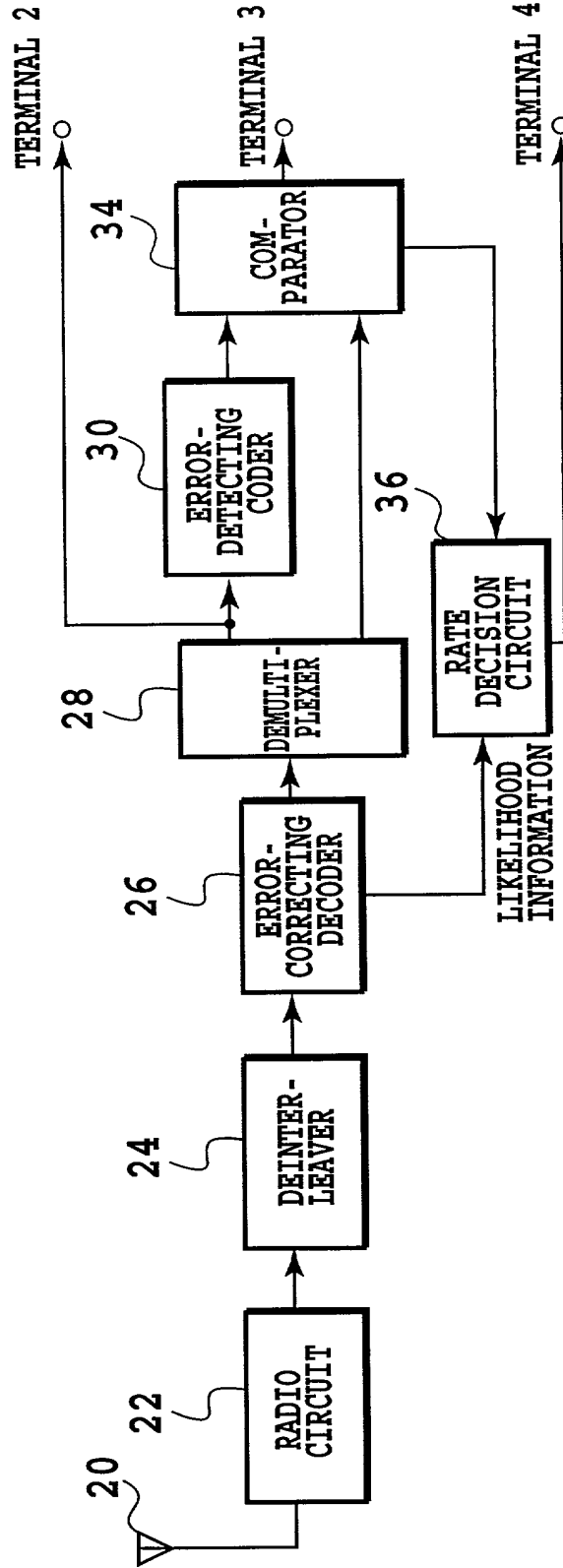


FIG.3B

RECEIVER CONFIGURATION

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OUTPUT OF MULTIPLEXER

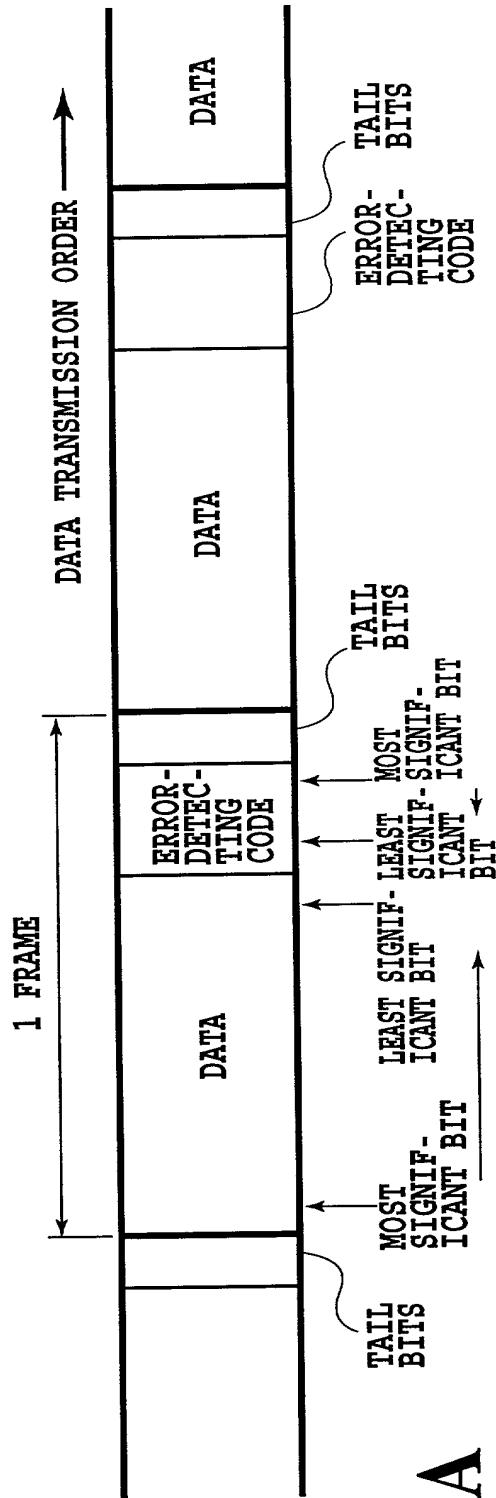


FIG. 4A

OUTPUT OF MULTIPLEXER

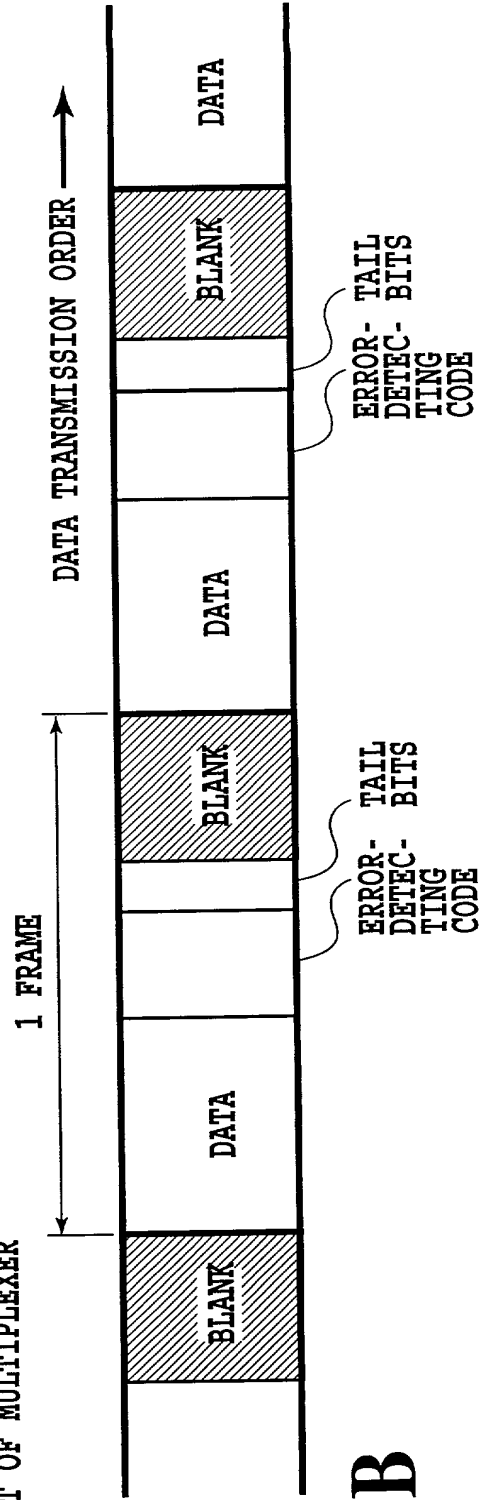


FIG. 4B

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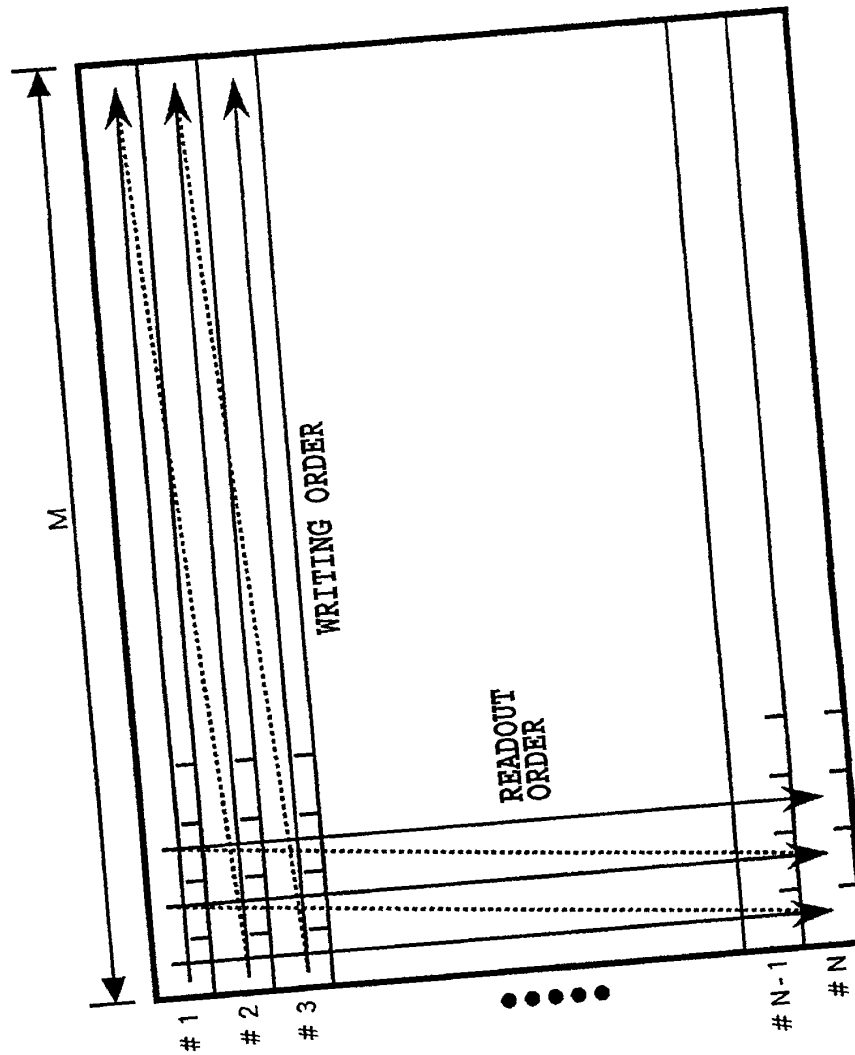


FIG.5

OUTPUT OF FRAME MEMORY

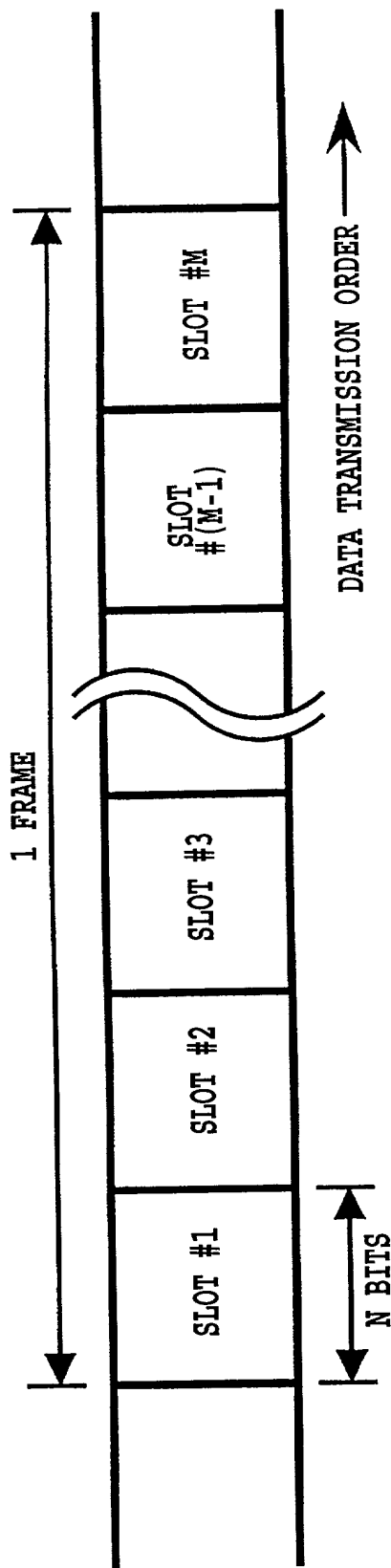


FIG.6

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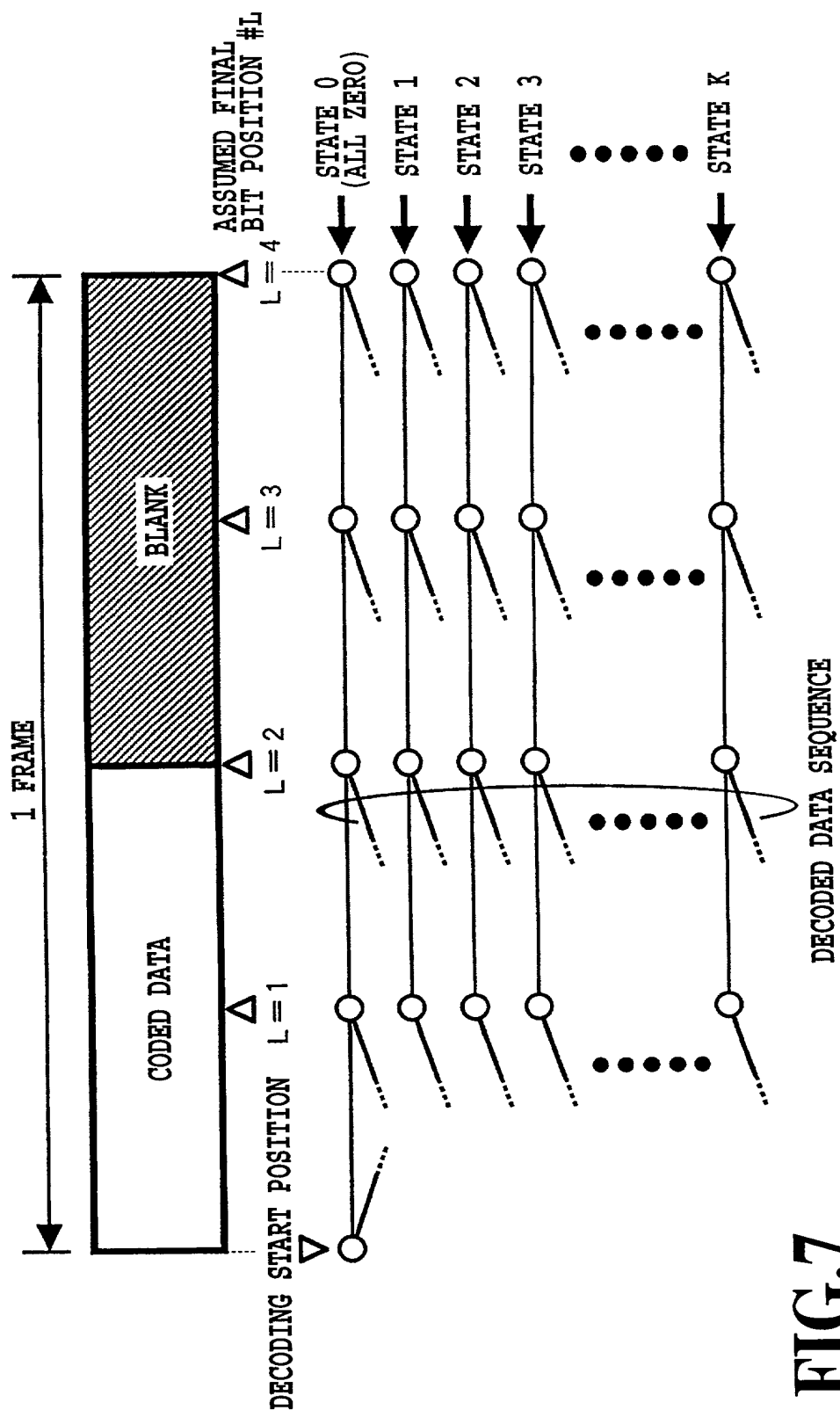


FIG. 7

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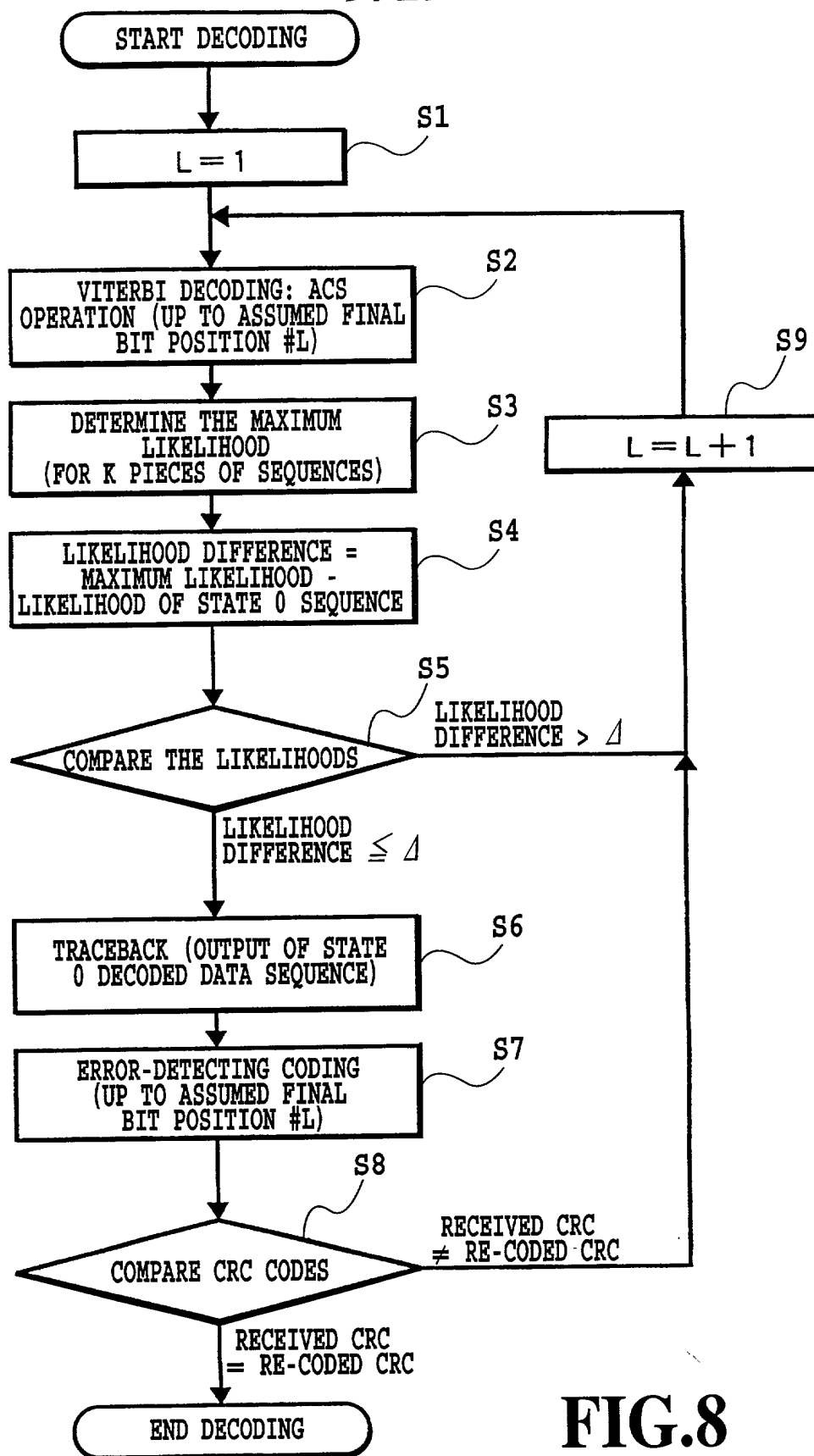
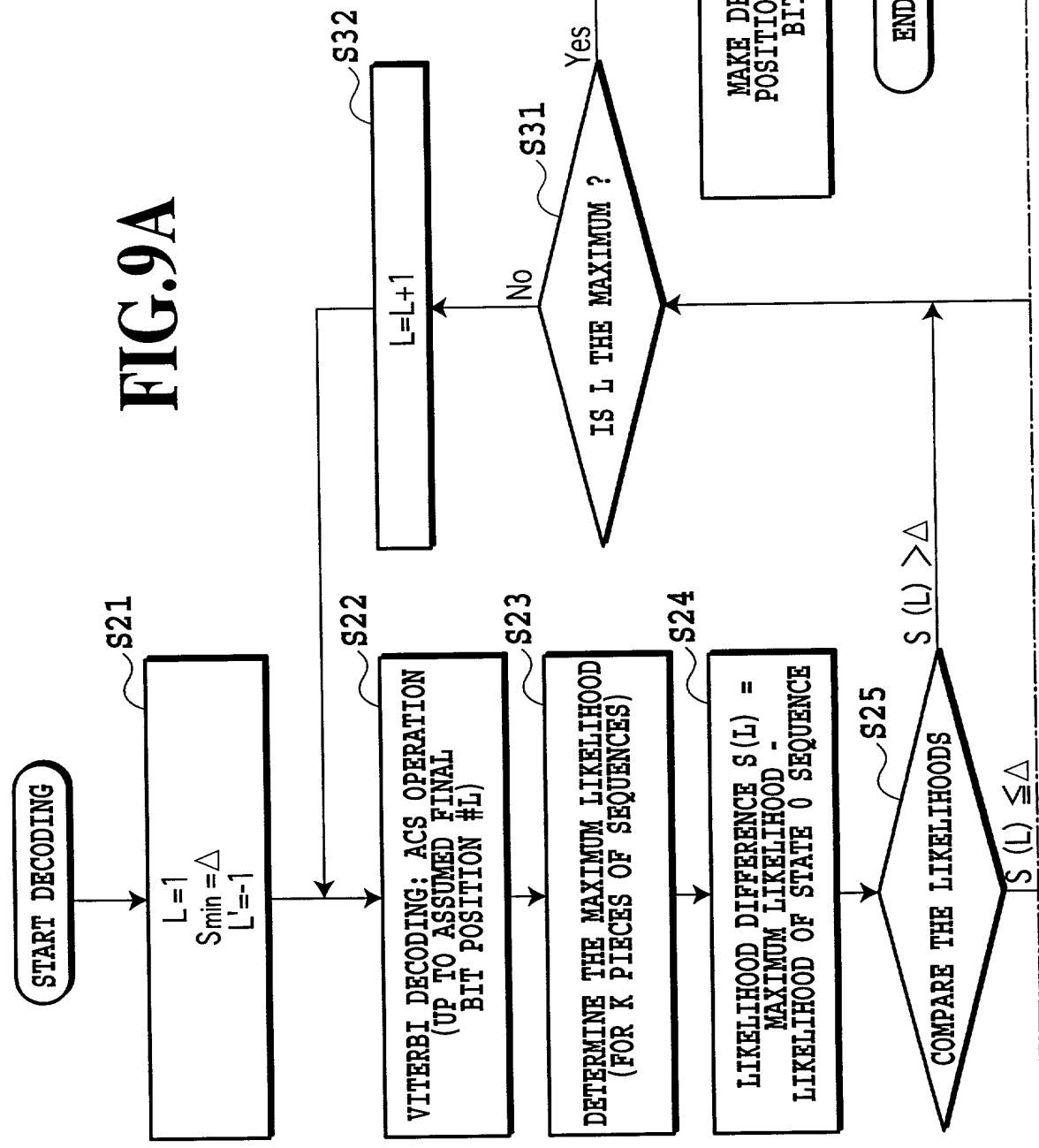


FIG.8

FIG.9
FIG.9A
FIG.9B



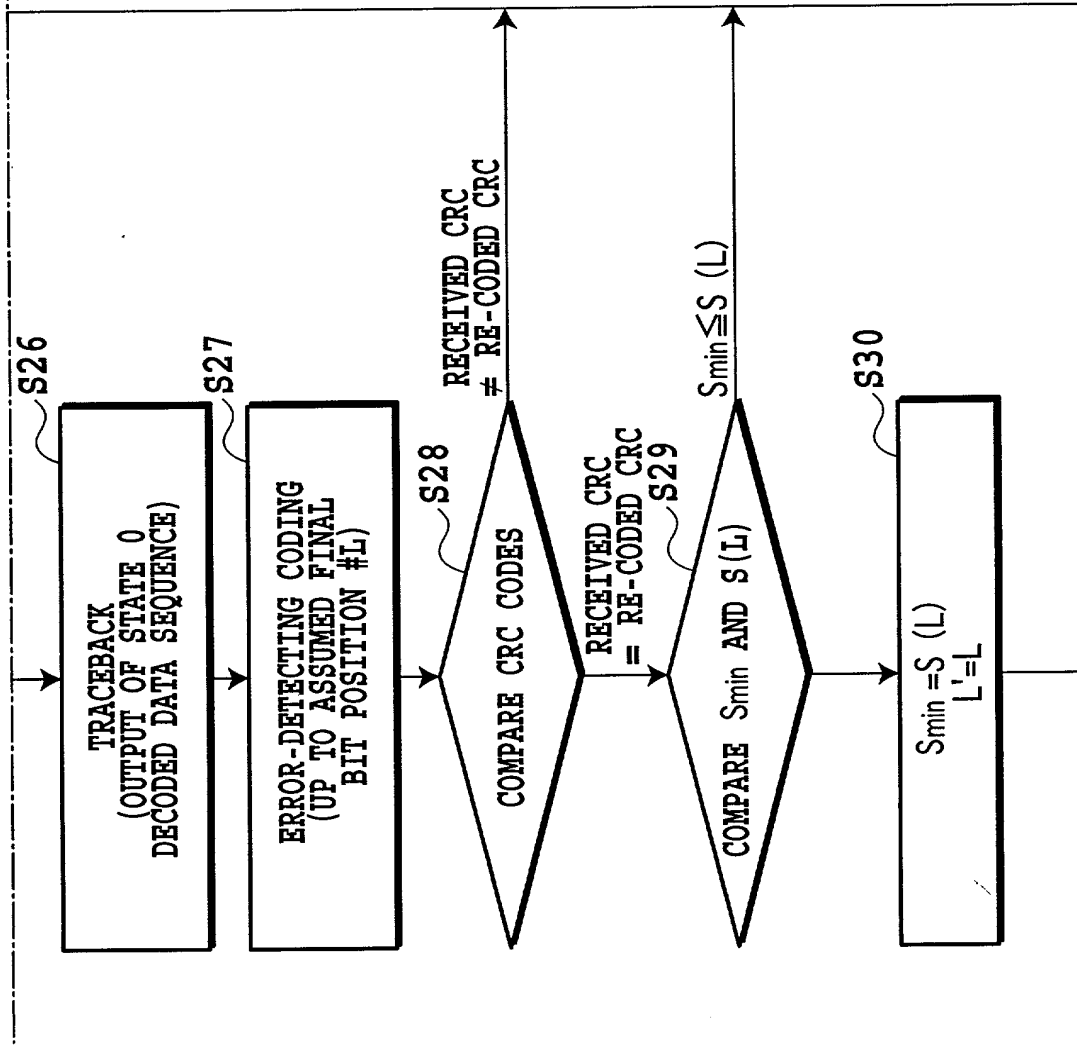
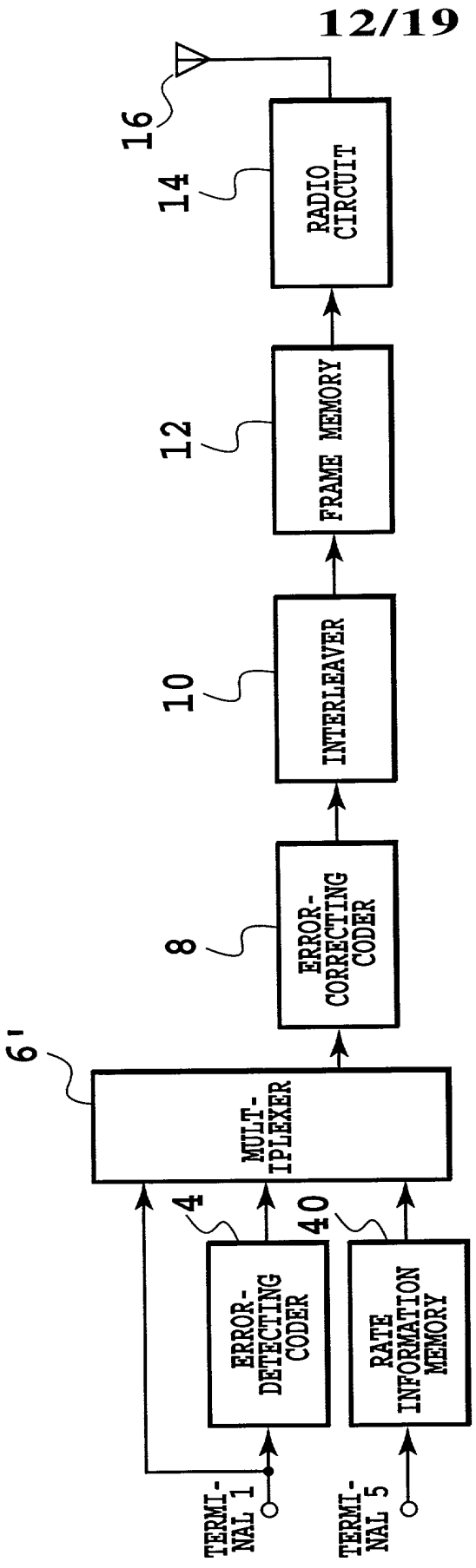


FIG.9B



TRANSMITTER CONFIGURATION

FIG.10A

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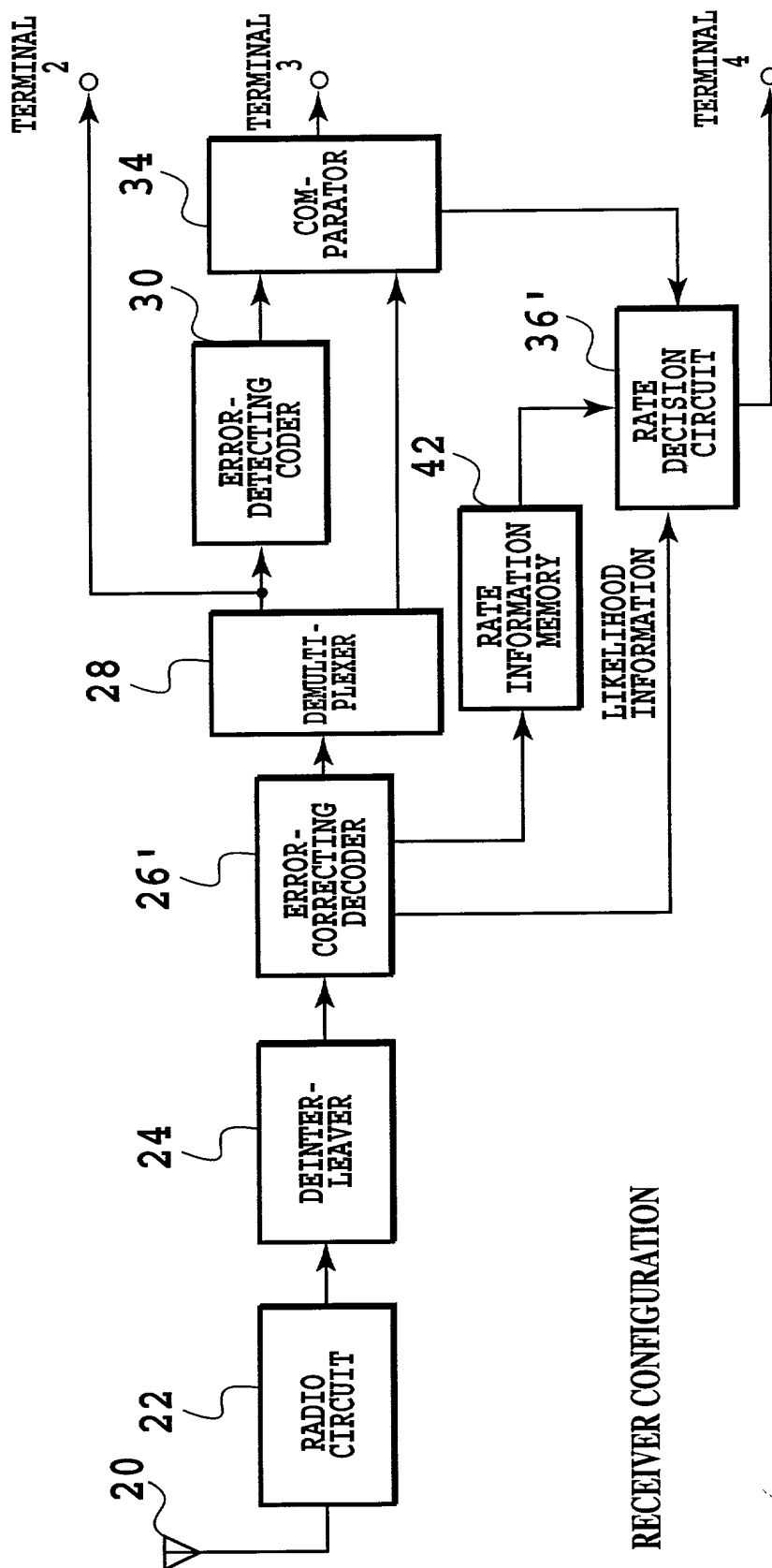


FIG. 10B

OUTPUT OF MULTIPLEXER

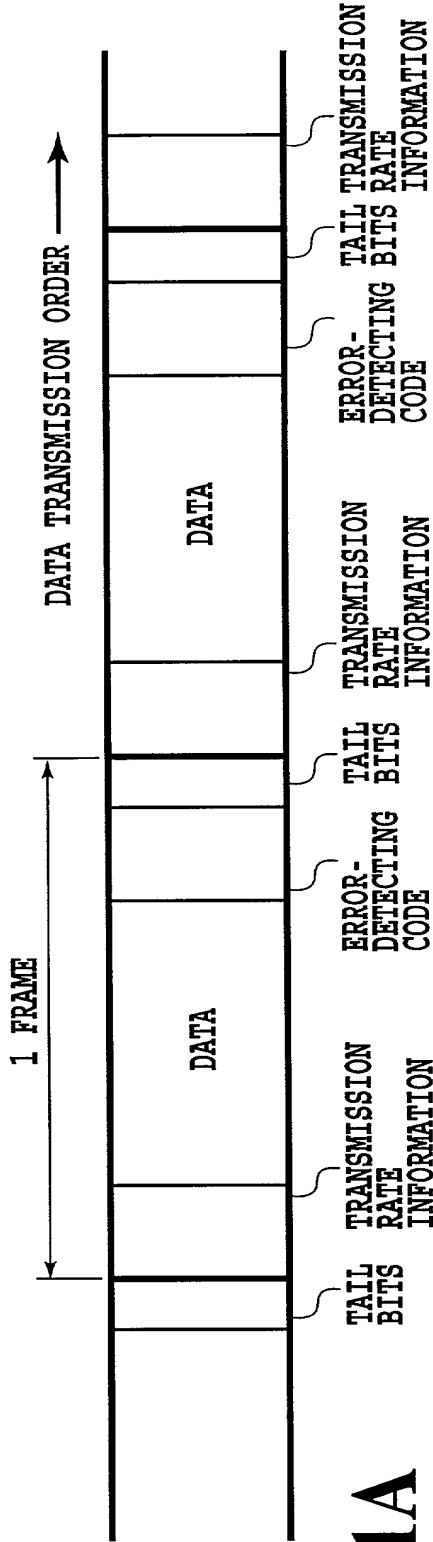


FIG. 11A

OUTPUT OF MULTIPLEXER

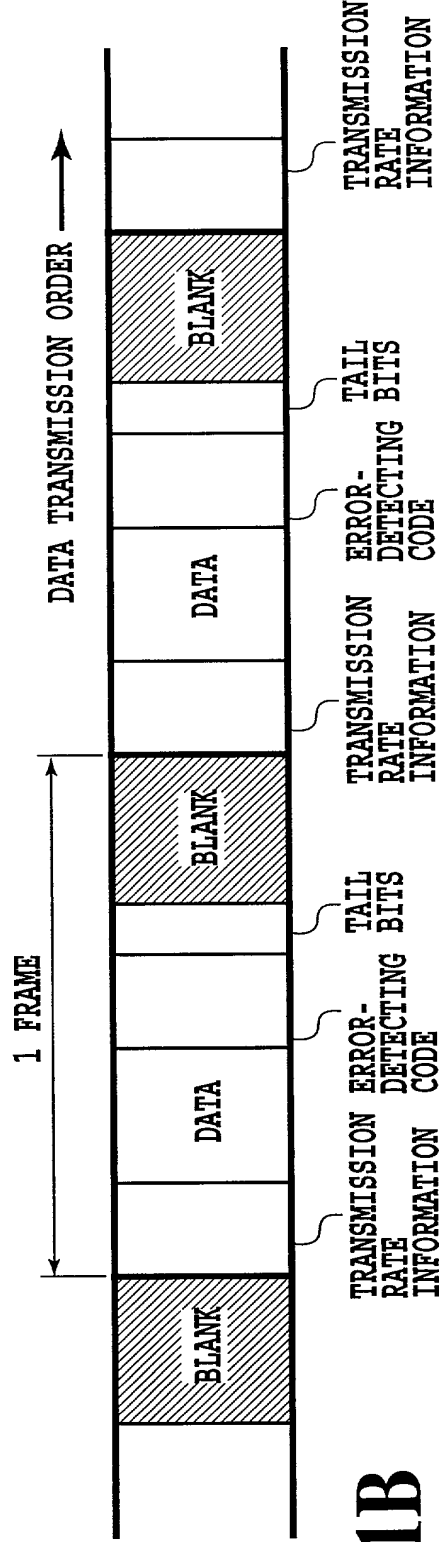


FIG. 11B

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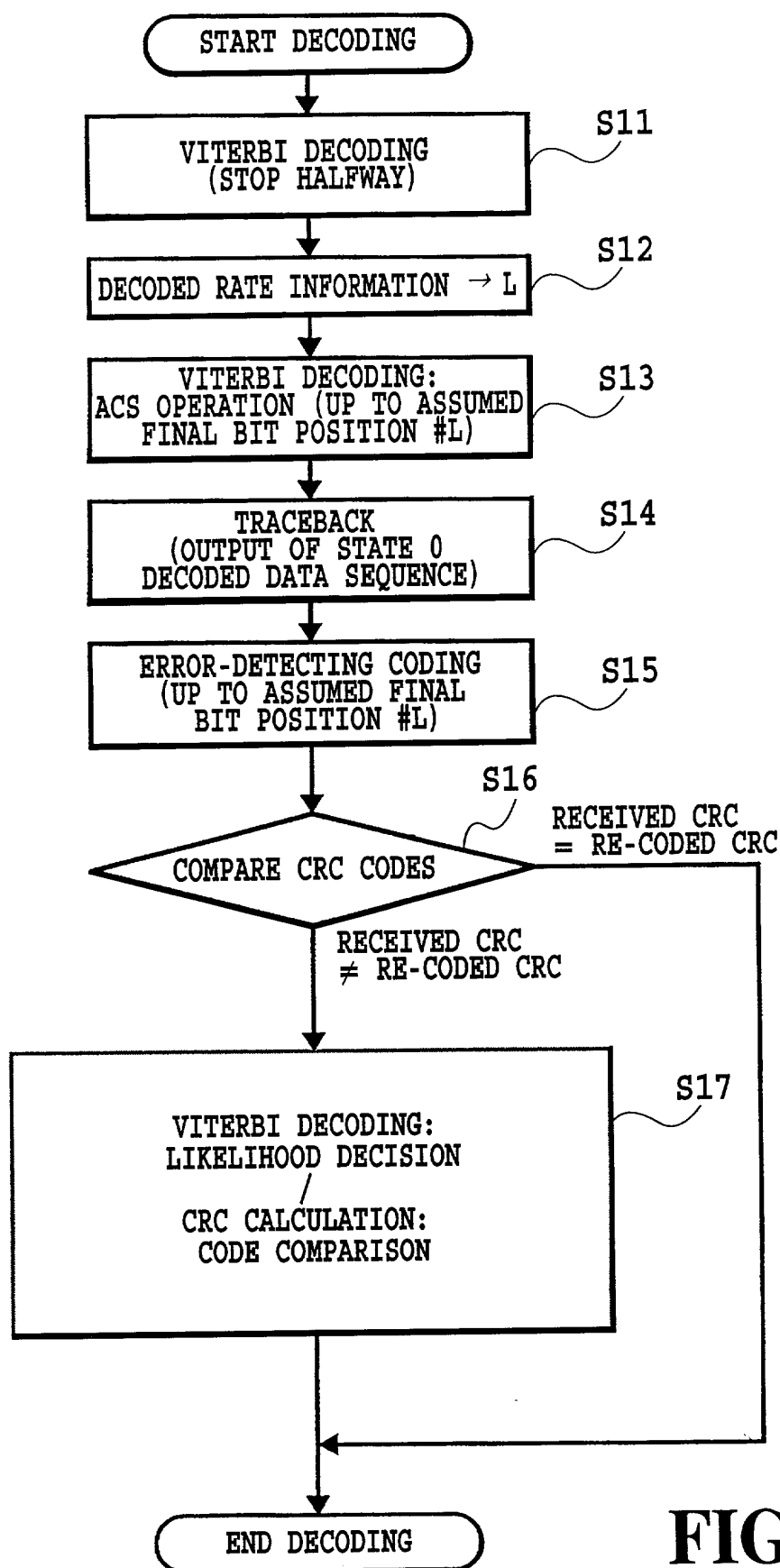


FIG.12

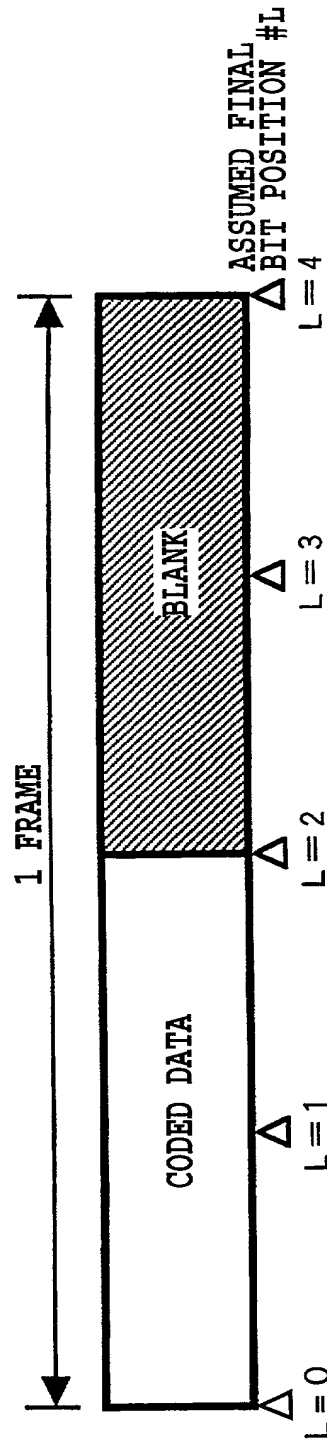


FIG.13

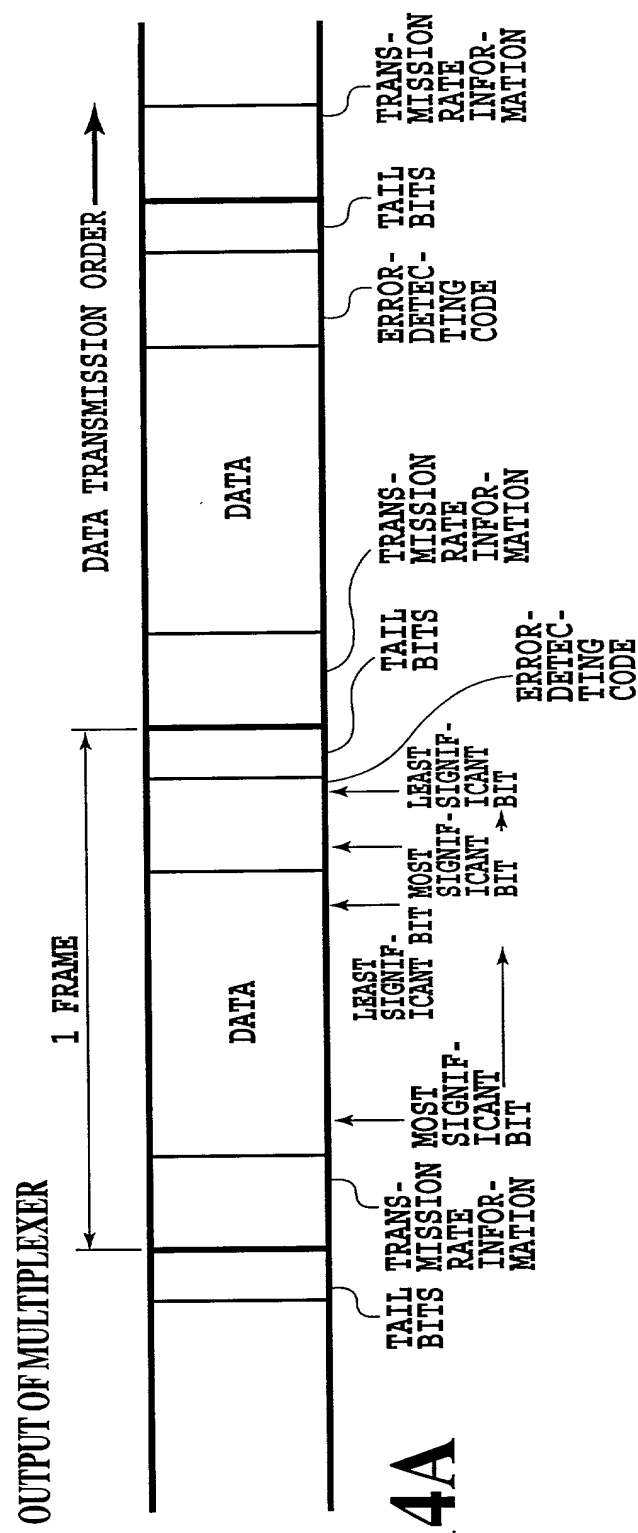


FIG.14A

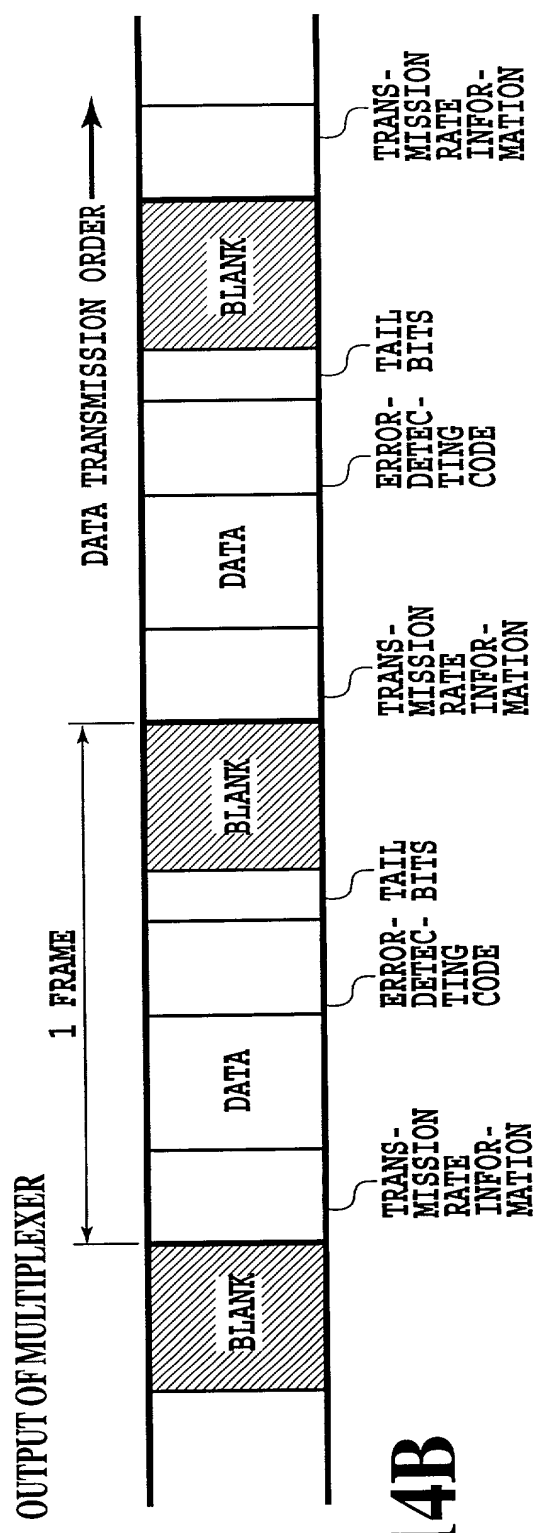


FIG.14B

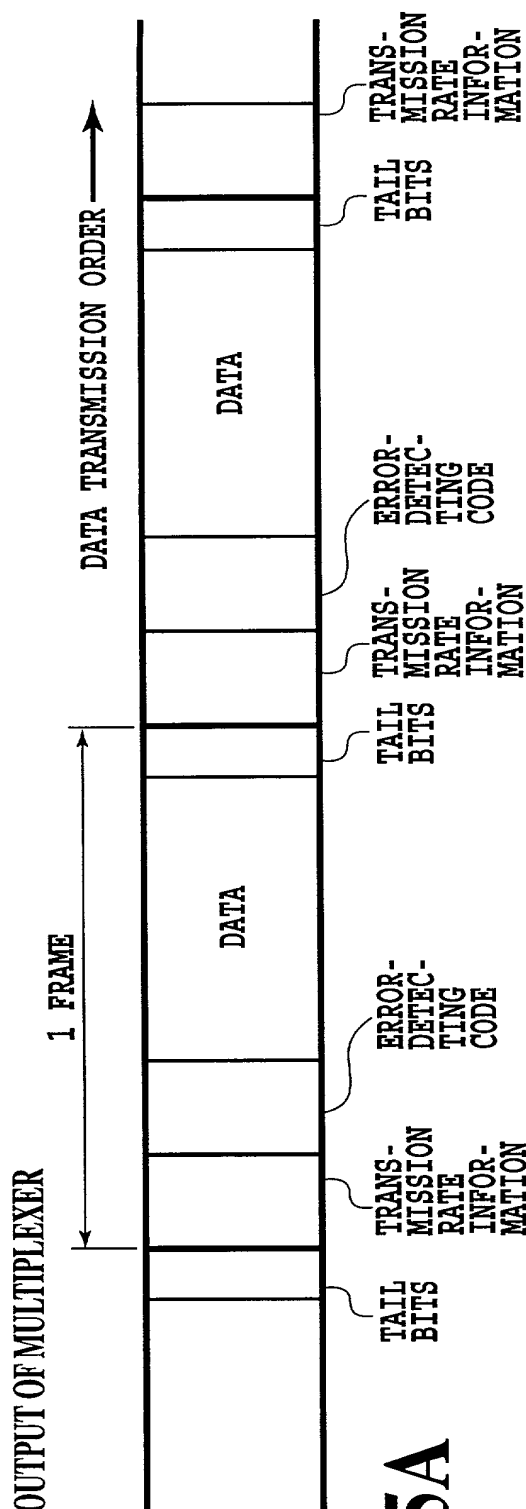


FIG.15A

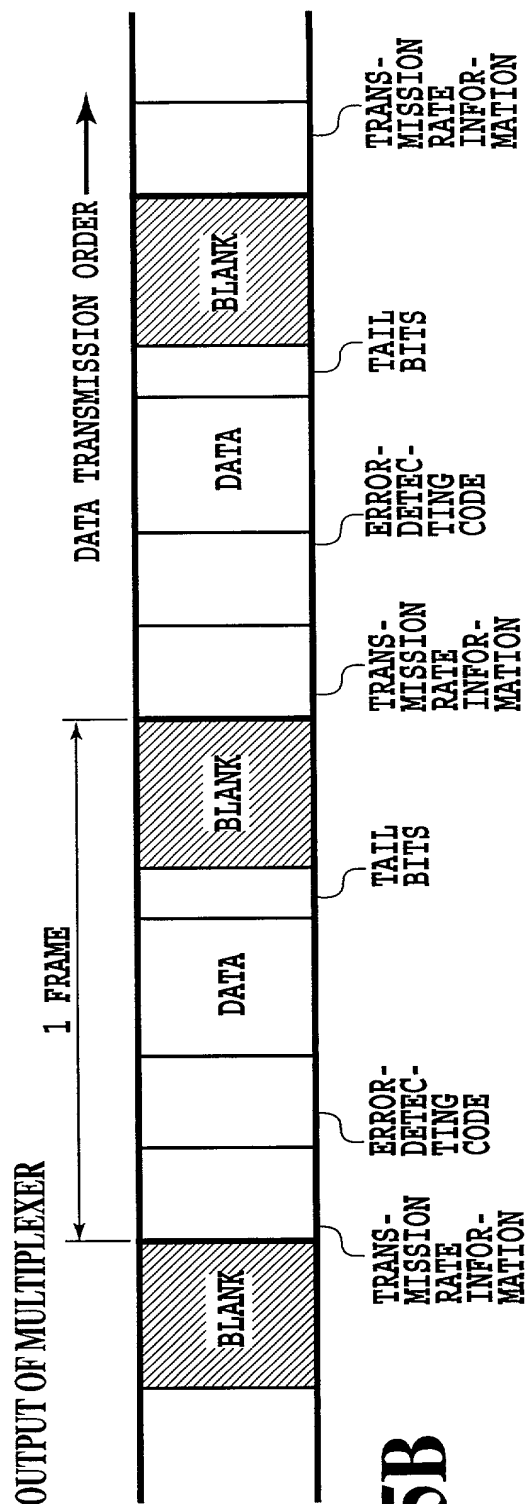


FIG.15B

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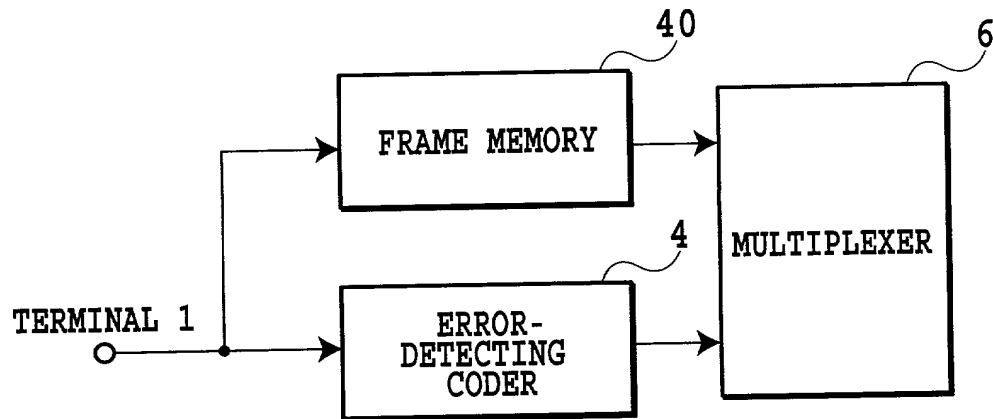


FIG.16A

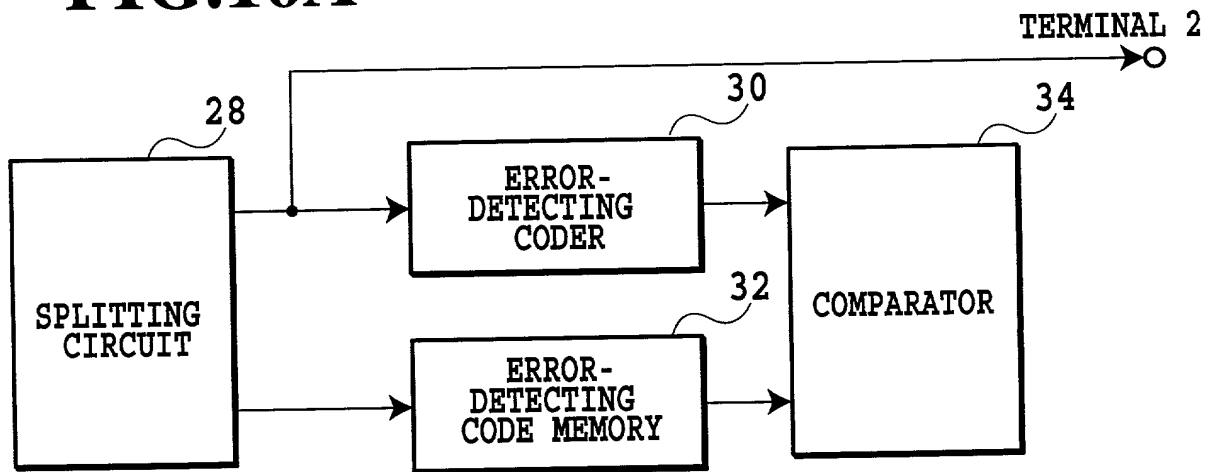


FIG.16B